WHAT IS CLAIMED IS:

1. A semiconductor substrate for use in a semiconductor device in which first device components are disposed on an insulating material and second device components are fabricated, wherein;

a thermal-oxide layer of 10 μm or more in thickness is formed in a region where the first device components are to be disposed, and a groove packed with a polycrystalline semiconductor is formed at an inward position from the peripheral edge of the thermal-oxide layer and along the same peripheral edge.

2. The semiconductor substrate according to claim 1, wherein said groove packed with a polycrystalline semiconductor has a depth larger than the thickness of said thermal-oxide layer.

3. The semiconductor substrate according to claim 1, wherein said semiconductor substrate comprises a silicon-on-insulator substrate, and said thermal-oxide layer reaches a buried oxide film layer of the silicon-on-insulator substrate.

4. The semiconductor substrate according to

claim 1, wherein said first device components comprise passive components, and said second device components comprise active components.

5. The semiconductor substrate according to claim 4, wherein said passive components comprise passive components that handle high-frequency signals.

6. A process for manufacturing a semiconductor substrate for use in a semiconductor device in which first device components are disposed on an insulating material and second device components are fabricated; the process comprising the steps of:

simultaneously forming, in a region in a semiconductor substrate in which region the first device components are to be disposed, a first groove of 10 μm or more in depth and, along the perimeter of a region where the first groove is to be formed, a second groove having a larger groove width than the groove width the first groove has;

making a thermal-oxide film grow by thermal oxidation, from the inner surfaces of the first and second grooves to make, in the first groove, the groove filled with the thermal-oxide film and form, in the second groove, the thermal-oxide film on the

bottom and sidewalls thereof leaving a third groove therein; and

packing the third groove with a polycrystalline semiconductor.

7. A process for manufacturing a semiconductor substrate for use in a semiconductor device in which first device components are disposed on an insulating material and second device components are fabricated; the process comprising the steps of:

simultaneously forming, in a region in a semiconductor substrate in which region the first device components are to be disposed, a plurality of first grooves of 10 μm or more each in depth in the state that they stand adjacent to each other, and, along the perimeter of a region where the first grooves are to be formed, a second groove having a larger groove width than the groove width the first grooves each have;

making a thermal-oxide film grow by thermal oxidation, from the inner surfaces of the first and second grooves to make, in the first grooves, the grooves filled with the thermal-oxide film and form, in the second groove, the thermal-oxide film on the bottom and sidewalls thereof leaving a third groove

therein; and

packing the third groove with a polycrystalline semiconductor.

8. The semiconductor substrate manufacturing process according to claim 6, wherein, in the step of forming a first groove and a second groove simultaneously, said second groove is formed in a depth larger than the depth of said first groove.

9. The semiconductor substrate manufacturing process according to claim 6, wherein the step of packing the third groove with a polycrystalline semiconductor comprises depositing a polycrystalline semiconductor on said semiconductor substrate to provide the polycrystalline semiconductor in the third groove, thereafter removing an excess polycrystalline semiconductor deposited at the surface portion of said semiconductor substrate, and then thermally oxidizing the polycrystalline semiconductor having remained in surface concavities of said semiconductor substrate.

10. The semiconductor substrate manufacturing process according to claim 6, wherein, where the groove width of said first groove is represented by W1,

the groove width of said second groove by W3, the difference in coefficient of thermal expansion between said semiconductor substrate and the thermal oxide thereof by A, the maximum width of a thermal-oxide film portion that is formed around said first groove accompanying thermal oxidation by W, and the difference in temperature between room temperature and maximum thermal oxidation treatment temperature by T, these satisfy the following expression:

$$W3 > \{(A \cdot W \cdot T)/2\} + W1.$$

11. The semiconductor substrate manufacturing process according to claim 6, wherein, in said first groove, the aspect ratio L1/W1 thereof which is the dimensional ratio of groove depth L1 to groove width W1 is 10 or more.

12. The semiconductor substrate manufacturing process according to claim 6, wherein, in said first groove, the aspect ratio L1/W1 thereof which is the dimensional ratio of groove depth L1 to groove width W1 is 20 or more.

13. The semiconductor substrate manufacturing process according to claim 6, wherein, in said first

groove, the groove width W1 thereof is 1 μm or less.

14. The semiconductor substrate manufacturing process according to claim 6, wherein a silicon-on-insulator substrate is used as said semiconductor substrate, and said first and second grooves are so formed as to reach a buried oxide film layer of the silicon-on-insulator substrate.

15. The semiconductor substrate manufacturing process according to claim 6, wherein said first device components comprise passive components, and said second device components comprise active components.

16. The semiconductor substrate manufacturing process according to claim 6, wherein said said passive components comprise passive components that handle high-frequency signals.

17. The semiconductor substrate manufacturing process according to claim 7, wherein, in the step of forming first grooves and a second groove simultaneously, said second grooves are each formed in a depth larger than the depth of said first groove.

18. The semiconductor substrate manufacturing process according to claim 7, wherein the step of packing the third groove with a polycrystalline semiconductor comprises depositing a polycrystalline semiconductor on said semiconductor substrate to provide the polycrystalline semiconductor in the third groove, thereafter removing an excess polycrystalline semiconductor deposited at the surface portion of said semiconductor substrate, and then thermally oxidizing the polycrystalline semiconductor having remained in surface concavities of said semiconductor substrate.

19. The semiconductor substrate manufacturing process according to claim 7, wherein, where the groove width of each of said first grooves is represented by W1, the groove width of said second groove by W3, the difference in coefficient of thermal expansion between said semiconductor substrate and the thermal oxide thereof by A, the maximum width of a thermal-oxide film portion that is formed around the first groove accompanying thermal oxidation by W, and the difference in temperature between room temperature and maximum thermal oxidation treatment temperature by T, these satisfy the following expression:

$W3 > \{(A \cdot W \cdot T)/2\} + W1$.

20. The semiconductor substrate manufacturing process according to claim 7, wherein, in each of said first grooves, the aspect ratio L1/W1 thereof which is the dimensional ratio of groove depth L1 to groove width W1 is 10 or more.

21. The semiconductor substrate manufacturing process according to claim 7, wherein, in each of said first grooves, the aspect ratio L1/W1 thereof which is the dimensional ratio of groove depth L1 to groove width W1 is 20 or more.

22. The semiconductor substrate manufacturing process according to claim 7, wherein, in each of said first grooves, the groove width W1 thereof is 1 μm or less.

23. The semiconductor substrate manufacturing process according to claim 7, wherein a silicon-on-insulator substrate is used as said semiconductor substrate, and said first and second grooves are so formed as to reach a buried oxide film layer of the silicon-on-insulator substrate.

24. The semiconductor substrate manufacturing process according to claim 7, wherein said first device components comprise passive components, and said second device components comprise active components.

25. The semiconductor substrate manufacturing process according to claim 7, wherein said said passive components comprise passive components that handle high-frequency signals.